Facile Four-Mask Processes for Organic Thin-Film Transistor Integration Structure With Metal Interconnect

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***Abstract*— To enable an organic thin film transistor (OTFT) technology for circuit integration, the passivation layer and subsequent interconnect metallization on top of the OTFT is vital. In this work, a modified SU8 formulation is developed for forming the passivation layer on top of the OTFT with small molecule organic semiconductor (OSC). Based on the single SU8 passivation layer, via holes for interconnect metallization are easily formed, and the whole integration structure can be completed with facile four-mask processes. The OTFTs exhibit high mobility (> 2 cm^2/V $\cdot$ s), low leakage ($< 10^{-11}$ A over the whole gate voltage range from 20 V to -30 V) at short channel length (8 μm), excellent uniformity and stable electrical properties during operation and storage. The results well prove that the process of the modified SU8 solution for passivation is compatible with the small molecule OSC layer, and formation of the via connection is reliable.**

***Index Terms*— Thin-film transistor, organic semiconductor, passivation, interconnect.**

I. Introduction

ATTRIBUTED to low temperature solution processability and excellent mechanical flexibility, the organic thin-film transistors (OTFTs) have been intensively studied for developing low cost flexible integrated circuits, active matrix backplanes for displays and sensors, and emerging truly flexible and stretchable electronics [1]–[6].

Solution printing of all the layers within an OTFT integration architecture could be able to fully explore the unique advantages of this technology. However, currently there is no industrialized process to stack the different layers accurately enough to achieve the required circuit performance and integration density. A compromise approach would be utilizing the existing flat panel display manufacturing processes, including sputtering, photolithography, wet/dry etching, spin or slot-die coating to scale up the OTFT processes for the required circuit performance at a relatively low cost [7]. For that, it is critical to minimize the required number of process steps and masks to pattern and stack all the layers with good processing compatibility.

In an integration architecture, instead of the source-drain electrode, organic semiconductor (OSC), organic gate insulator (OGI), and gate metal layers, the passivation layer and subsequent interconnect metallization is also key. Various OTFT architectures have been developed in the past for active matrix display backplanes and circuit integration [8]–[10]. To conveniently form via holes for metal interconnection between layers, a photo-patternable polymer is often adopted for the passivation layer. However, the OSC layer is sensitive to the chemical solvent used in processing of these photo-patternable polymers, especially for small molecule OSCs, which have higher mobility and higher purity compared to polymer counterparts. To address this issue, one additional layer using orthogonal solvent (e.g. fluoropolymer derivatives [8], water soluble polyvinyl alcohol (PVA) [10]) was coated on top of the OSC layer to protect it from processing the photo-pattenable polymer layer. However, dry etching of both layers simultaneously using one photomask for reliable via connection is challenging, since the higher rate of dry etch of the underlying layer might cause undercutting of the upper photo-patternable layer. Therefore, such a bi-layer structure might add significant cost by using extra materials and more complex etching processes, and also cause variability in the via connections.

In this work, an OTFT integration architecture based on high mobility small molecule OSC is developed by adopting SU8, a popular photoresist, for the passivation layer. For SU8, the commonly used solvent is cyclopentanone, which is incompatible with the small molecule OSC. Instead of adding an additional protection layer, the SU8 solution is modified with dihydrolevoglucosenone (Cyrene^{TM}, Circa, AUS) as the solvent for the passivation layer. Cyrene is a non-toxic solvent derived from cellulose. With such a modified SU8 formulation to form the passivation layer, no additional protection layer is needed, and the whole OTFT integration architecture is able to be completed with facile four mask processes. The fabricated OTFTs exhibit high mobility, low leakage at short channel length (8 μm), excellent uniformity, and stable electrical properties during operation and storage.

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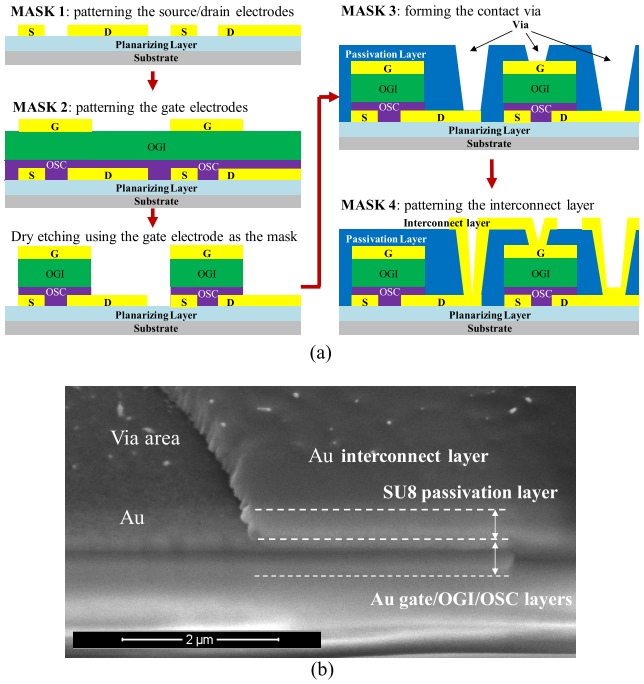

Fig. 1. (a) Illustration of the four-mask process flow for fabrication of the OTFT integration architecture with metal interconnect: the 1st mask for patterning the source/drain (S/D) electrodes, the 2nd mask for patterning the gate (G) electrodes; the 3rd mask for forming the contact via, and the 4th mask for patterning the metal interconnect layer. (b) The scanning electron microscopy (SEM) image showing the cross-sectional structure of the fabricated OTFT integration structure.

II. Experimental

OTFTs were fabricated in the top-gate bottom-contact (TGBC) configuration on either glass or plastic substrates as shown in Fig. 1(a). Polymer resin (ES2110, Zeon) was spin-coated and then cross-linked by baking at 150 °C to form the planarizing layer. Gold (Au) source-drain electrodes (50 nm thick) were deposited by sputtering, followed by photolithography and wet etching processes. The sample surfaces were then treated by oxygen plasma to increase surface energy for further processes. A self-assembled monolayer (SAM) of 3-fluoro-4-methoxythiophenol (Fluorochem, UK) was deposited from a 10 mM solution in 2-propanol. Two subsequent cycles of 2-propanol deposition and spin-coating were used to rinse any excess thiol from the surface. After baking the substrate at 100°C for 1 minute, the organic semiconductor (OSC) solution of a small molecule semiconductor and a high-k polymer semiconductor binder was spin-coated at 500 rpm for 10s followed by 1000 rpm for 60s followed by a further bake at 100°C for 60s. Cytop CTL-809M diluted to 4.5% solids was spin-coated to obtain an about 300 nm thick film as the gate dielectric layer, providing specific gate capacitance of 6 nF/cm^2. The gate electrode layer of 50 nm thickness was deposited by thermal evaporation, and patterned using photolithography and wet etching. The unwanted areas of the OSC and OGI layers were removed by oxygen RIE plasma etching using the gate metal as a hard-mask.

For the encapsulation layer, the modified SU8 formulation was made at 10% overall solid concentration in a mixed solvent of Cyrene^{TM}: isopropanol in 9:1 by weight, and a photoacid triarylsulfonium hexafluoroantimonate at 10% by weight of the SU8. The SU8 formulation was spin-coated at 2000 rpm for 30 s and pre-baked at 95 °C

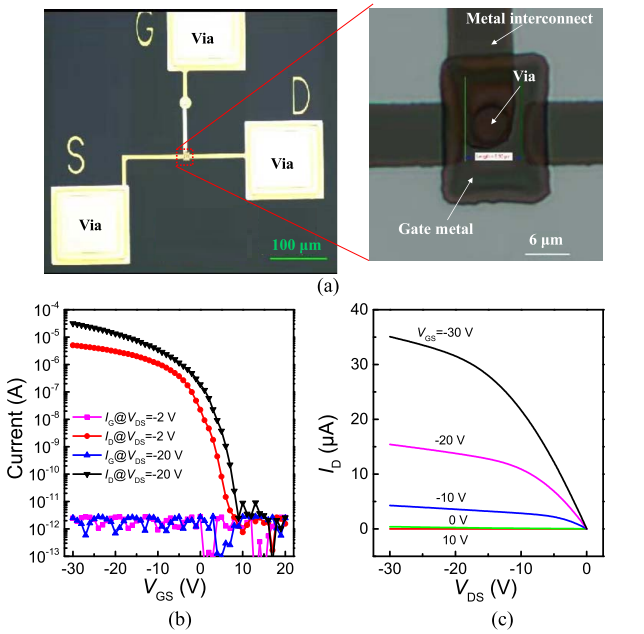

Fig. 2. (a) Top-view optical microscopy image of the fabricated OTFT integration structure. (b) Measured transfer characteristics (I_D-V_{GS}) and the gate leakage (I_G) versus V_{GS} of the OTFTs in the structure. (c) Measured output characteristics (I_D-V_{DS}) of the device.

for 2 minutes, resulting in a layer of about 480 nm thickness. Via holes through the SU8 layer for metal interconnection were formed by processes of photolithography, baking (95 °C for 2 minutes) and developing using Microposit^{TM} EC solvent (Rohm and Haas). Finally, a 50 nm Au interconnect layer was sputtered and patterned using photolithography to create electrical connections where required. The scanning electron microscopy (SEM) image in Fig. 1(b) shows the cross-sectional structure of the fabricated OTFT integration structure with the metal interconnect layer, the via and the passivation layer.

The devices were characterized with a Keithley 4200 semiconductor characterization system in air ambient.

III. Results and Discussions

The top-view optical microscopy image of the fabricated OTFT integration structure is shown in Fig. 2(a). The measured typical transfer (I_D-V_{GS}) and output (I_D-V_{DS}) characteristics of the OTFTs in the fabricated integration structure are given in Fig. 2(b) and (c), exhibiting proper field effect transistor behaviors. The extracted apparent mobility in the linear regime (μ_{lin}) is about 2.23 cm^2/V.s, which is one of the best results for short channel (<10 μm) OTFTs [6]. The devices present high ON/OFF ratio larger than 10^6, and the gate leakage current (I_G) is well below 10^{-11} A over the whole V_{GS} sweeping range from 20 V to −30 V. Since the measurable lowest level of the current is limited by the leakage and noise of the test equipment, the actual drain and gate leakage current should be even lower. Such low leakage characteristics are attributed to the well patterned OSC layer in the structure eliminating the parasitic leakage paths outside the channel region [11], [12]. Using the gate electrode as the hard mask for patterning the organic semiconductor layer leads to a simplified lithography process.

Fig. 3(a) gives the measured I_D-V_{GS} characteristics of 12 devices on the substrate, showing very good uniformity. Constant voltage bias stress test was carried out to

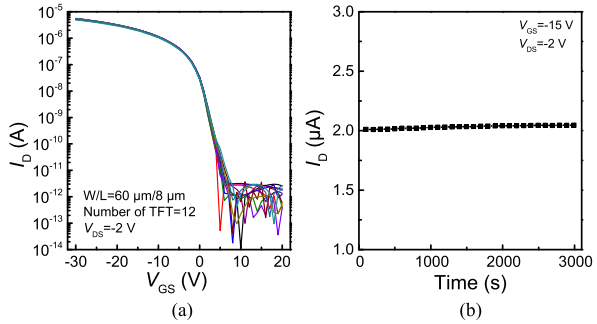

Fig. 3. (a) The measured I_D-V_{GS} characteristics of 12 devices on the substrate, showing very good uniformity. (b) The measured I_D over time at constant voltage bias of $V_{GS} = -15$ V and $V_{DS} = -2$V for 3000 s. The device has a channel width of 60 μm and channel length of 8 μm.

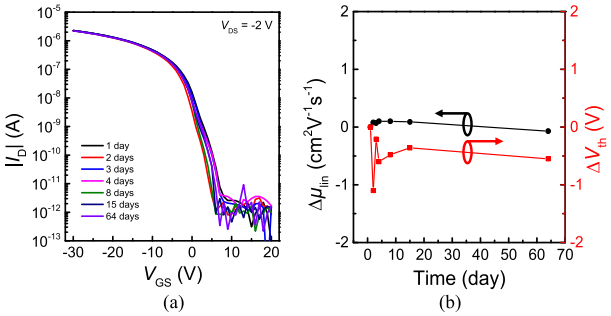

Fig. 4. (a) The measured transfer characteristics of the device stored in the ambient air environment for 64 days. (b) The relative changes of extracted μ_{sat} and V_{th} of the devices versus the storage time. The device has a channel width of 12 μm and channel length of 8 μm.

study the operational stability of the device. As shown in Fig. 3(b), at constant voltage bias of $V_{GS} = -15$ V and $V_{DS} = -2$V, the device is able to maintain nearly constant I_D of 2 μA for 3000 s. At the device level, the low-k non-polar Cytop gate dielectric layer helps to form low interfacial trap density, which is important for achieving the excellent bias-stress stability [13]–[15]. The measurements utilize the contacts on the metal interconnect layer, which connect to the source/drain/gate electrodes of the OTFT through the via holes. The excellent uniformity and stability in Fig 3 and good device performance in Fig. 2 also prove that the process of the SU8 passivation layer with Cyrene solvent and formation of the via connection is reliable, and compatible with small molecule OSC layer.

Fig. 4(a) shows the measured I_D-V_{GS} characteristics of the device at different time when it being stored in an ambient environment for 65 days. The extracted changes of μ_{lin} and V_{th} over time are given in Fig. 4(b). Stable electrical properties of the device during storage in ambient environment can be seen. These results prove that with the single SU8 passivation layer, such an integration structure can effectively suppress the possible ambient influence.

IV. Conclusion

An OTFT integration structure with facile four-mask processes, using the gate electrode as the hard mask for patterning the organic semiconductor layer, is developed in this work. By using Cyrene as solvent to modify the SU8 formulation, it can be used to form the passivation layer without additional protection layer for OTFTs with small molecule OSC. Therefore, the via hole can be easily formed, and four-mask processes are able to be developed for the integration structure. The fabricated short channel (8 μm) OTFTs with small molecule OSC in the structure exhibits high mobility, low leakage, and excellent uniformity and stability of the electrical properties. The reliability of the passivation layer and via formation processes is well proved by these experimental results. It would provide a facile approach for developing high performance circuit integration with solution processed OTFTs.

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